



64 CHANNEL WIDE I/O PERIPHERAL CARD

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I. Features

- 64 channel digital I/O configurable in 8 channel blocks
- In-system FLASH programmable Philips P89C51RD+ microcontroller
- In-system Altera EPM7128S programmable logic array port controller
- Flexible component areas for pull-up/-down, and high current drive (eg 250mA 12V)
- Flexible connector arrangements for 0.1" IDC or 3.5mm terminal strip connections
- Jumper configuration for common GND, +5V or +12V terminal pairings
- Battery backed RAM expansion capability
- Multi-module expansion capability allowing up to 256 or more I/O channels
- RS232 serial port for programming and application use
- Single supply (12V) operation
- Single Eurocard format

II. General Description

The card consists of 64 channels of digital I/O port arranged in 8 blocks of 8 channels controlled by an ISP (in-system programmable) Flash microcontroller cpu on a single Eurocard format pcb. The I/O port expansion is handled in an ISP FPGA (field programmable gate/logic array) to allow for flexible system reconfiguration and upgrade. Each block of 8 channels can be independantly configured to be an input block or output block (with the exception of block1 which is input only). The blocks have a flexible architecture pcb footprint area that allows for a variety of component configurations to be fitted:

- pull-up or pull-down resistors
- series current limiting resistors
- R-C-R filter components
- relay or lamp sink drivers
- relay or lamp source drivers
- clamp diodes

Inputs for example, could have pull-ups to allow switch closures to be simple pull-to-grounds, have some current limit protection in the form of series resistors and, if required, diode clamps to prevent overvoltage at the device port. Outputs could direct drive LEDs with series resistors or, for higher power or voltage requirements, have ULN2803 o/c darlington sink drivers fitted for driving relays or lamps at 12V 250mA capability. (Alternatively outputs may be "source" driven with the UDN2981 device.) A pair of jumpers per block allow for the pin out variations of these different components.

The I/O block connections are also flexible and one of two types of connectors can be fitted:

16 pin IDC header 0.1"

16 way 3.5mm terminal strip - screw type or pcb disconnect

Pairs of connections are provided for each I/O channel for the signal ("A") and its return GND or voltage source ("B"). The 8 B connections in each block are commoned together and may be connected to GND, the +5Vdrive rail, the +12Vdrive rail or some externally provided higher voltage supply (typ. 50V max). A pair of jumpers per block select the appropriate connection. The "drive" rails are diode isolated from the main electronics power supply and protected by resettable fuses

The I/O port expander is implemented in an Altera EPM7128S in-system programmable logic array. (Optionally the EPM7160S 160 macrocell array may be fitted for more complex embedded functionality). The device may be reconfigured with the downloading of programming files through a 10-pin header using a suitable Altera "ByteBlaster" adaptor.

The microcontroller used on the board is the Philips P89C51RD+ which has 64KB of on-chip Flash programmable ROM and 1KB of RAM. A mezzanine header arrangement allows the RAM on-board to be expanded with up to 32KB of battery backed RAM (or the potential attachment of other daughter modules types). The device contains the software for a simple boot loader which handles the erasing and reprogramming of the main code ROM via an RS232 serial interface (9D socket connector, DCE pinout). The on-board serial interface may be used for other application based functions when not in use for programming. Programming mode is entered on power-up based on an accessible switch setting. Circuitry is also present for the enabling and disabling of the Vpp programming voltage under processor control allowing in-application programming utilities to be developed.

A further 32/34 way expander connector is provided to allow for up to 3 additional boards in multiple board configurations. The connector location may take either a 34pin IDC header connector (for applications where the expansion is handled through a ribbon cable harness) or a 32 pin 1/2 size DIN41612 connector (where the application has cards slotted into a small backplane). The additional expansion modules would not have their cpu's fitted but could be fitted with RAM or other daughter modules.



III. I/O Configurations

The 8 blocks of I/O areas are flexible and can take a variety of different components in a number of configurations.

The 10pin single-in-line location UPn can take SIP resistor packs, diode arrays or similar and, depending on orientation, be set to pull-up or pull-down or clamp to +5V or GND.

The 20pin DIP location PDn can be fitted with shorting links, series resistor packages, R-C-R filter network packages, high current relay/lamp sink drivers (e.g. ULN2803), high current relay/lamp source drivers (e.g. UDN2981) and potentially other components with similar pinout format.

The 10pin single-in-line location RPn can take SIP resistor packs, diode arrays or similar and, depending on orientation, be set to pull-up or pull-down or clamp to +5V or GND.

PLn is an 8x2 0.1" pin header area for external connections via IDC ribbon cables, for example.

A_JPn and B_JPn are for external connections via 3.5mm terminal strips for discrete wire terminations using screw or pcb disconnect methods. The terminal strips are connected in parallel with the 0.1" header and may be fitted instead of, but not as well as, the IDC header.

Typical usage of this area is shown in the examples below.

1 Switch closure input with pull-up (2K2) and series limiting resistor (220R). Switch closure pulls i/p to GND through jumper BW/B. Pin 1 of 16 pin series resistor pack fitted in pin 2 of 20pin PD location. Jumpers AW, CW, DW not fitted.

2 Direct digital (TTL level) input through R-C-R filter. Bourns 4120R fitted in PD location which has pins 1 and 20 to GND. Jumpers BW/B, CW/B and DW/B also connect to GND. Jumper AW not fitted.

3 Direct output drive to LED cathode. Series resistor (360R) sets LED current at approx. 10mA. LED anode connected to +5V through BW/A and AW/B. Pin 1 of 16 pin series resistor pack fitted in pin 2 of 20pin PD location. Jumpers CW, DW not fitted.

4 High current lamp output drive using ULN2803A open-collector darlington sink driver. "High" side of lamp connected to +12V through BW/A and AW/A. Low side pulled to GND through DW/B. (Flyback clamp diode integral part of ULN2803 to +12V through CW/A only really required for inductive loads)

5 High current relay output drive using ULN2803A open-collector darlington sink driver. "High" side of relay connected to +12V through BW/A and AW/A. Low side pulled to GND through DW/B. Flyback clamp diode integral part of ULN2803 to +12V through CW/A.

IV. Appendix 1: specifications

Size:

160mm x 100mm (single Eurocard)

Power supply:

200mA typ 12V DC unloaded
4A max @ 12V on-board load

I/O channels:

64 configurable in blocks of 8
Up to 64 i/p
Up to 56 o/p and 8 i/p

Output drive:

Direct
20mA any one output
750mA total board load
ULN2803A
500mA any one output
2A total load any one device
4A @ 12V total board output load (without external supply)
External supply to +50V

CPU:

Philips P89C51RD+ ISP Flash Microcontroller
64KB ROM, 1KB RAM expandable with mezzanine adaptor

Ports:

Altera EPM7128S ISP logic array.
(optional EPM7160S logic array)

Serial i/f:

RS232 DCE pinout via 9pin D-type socket

V. Appendix 2: Connector Pinout Allocation

JP1 - 0.1" 10 pin header - Altera ByteBlaster programming

1 TCK
2 GND
3 TDO
4 Vcc
5 TMS
6
7
8
9 TDI
10 GND



JP2 - 34 pin 0.1" header - Bus/module expansion (also J4 1/2 DIN41612)

1 Vcc
2 GND
3 AD1
4 AD0
5 AD3
6 AD2
7 AD5
8 AD4
9 AD7
10 AD6
11 GND
12 A15
13 A14
14 A13
15 A12
16 A11
17 A10
18 A9
19 A8
20 GND
21 ALE
22 /WR
23 /RD
24 /INT1
25 /INT0
26 RST
27 GND
28 CLK
29 +12VIN
30 Vcc
31 GND
32 GND
33 P1.0**
34 P1.1**

**Note - not available on J4

JP3 - 2mm MicroSpox - I2C (optional fit)

1 GND
2 Vcc
3 SCL
4 SDA

JP4 - 0.1" Molex - DCin (optional fit)

1 +12V
2 +12V
3 GND
4 GND

JP5**, JP6, JP8**, JP9 - 10 pin 0.1" Mezzanine Headers

(**Note JP5 and JP8 are placed to form a 20 pin 0.1" header pair)

JP5

1 Vcc
2 P0.0 AD0
3 P0.1 AD1
4 P0.2 AD2
5 P0.3 AD3
6 P0.4 AD4
7 P0.5 AD5
8 P0.6 AD6
9 P0.7 AD7
10 GND

JP6

1 /RAMCS
2 P1.0
3 P1.1
4 P1.2
5 P1.3
6 P1.4
7 P1.5
8 P1.6
9 P1.7
10 GND

JP8

1
2 P2.0 A8
3 P2.1 A9
4 P2.2 A10
5 P2.3 A11
6 P2.4 A12
7 P2.5 A13
8 P2.6 A14
9 P2.7 A15
10 GND

JP9

1 ALE
2 P3.0 RXD
3 P3.1 TXD
4 P3.2 /INT0
5 P3.3 /INT1
6 P3.4
7 P3.5
8 P3.6 /WR
9 P3.7 /RD
10 GND

JP7 - 0.156" Molex - DCin

1 +12V
2 GND

JP15 - 0.1" 10pin header - FPGA Port 5 internal

1
2 P5.0



- 3 P5.1
- 4 P5.2
- 5 P5.3
- 6 P5.4
- 7 P5.5
- 8 P5.6
- 9 P5.7
- 10 GND

SK1 - 9D socket - RS232 Serial DCE pinout

- 1
- 2 TxD (o/p)
- 3 RxD (i/p)
- 4
- 5 GND
- 6
- 7 /CTS (i/p)
- 8 /RTS (o/p)
- 9

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